Channel Link Demonstration Kit User Manual

P/N CLINK3V28BT-85

Rev 2.1

Interface Products

Table of Contents

Introduction:

National Semiconductor - Interface Products Group Channel Link evaluation kit contains a Transmitter (Tx) board, a Receiver (Rx) board along with interfacing cables. This kit will demonstrate the Channel Link chipset transmitting data streams using Low Voltage Differential Signaling (LVDS).

The Transmitter board accepts LVTTL/LVCMOS data signals from an incoming data source along with the clock signal. The LVDS Transmitter converts the LVTTL/LVCMOS parallel lines into four serialized LVDS data pairs plus a LVDS clock. The serial data streams toggle at 3.5 times the clock rate.

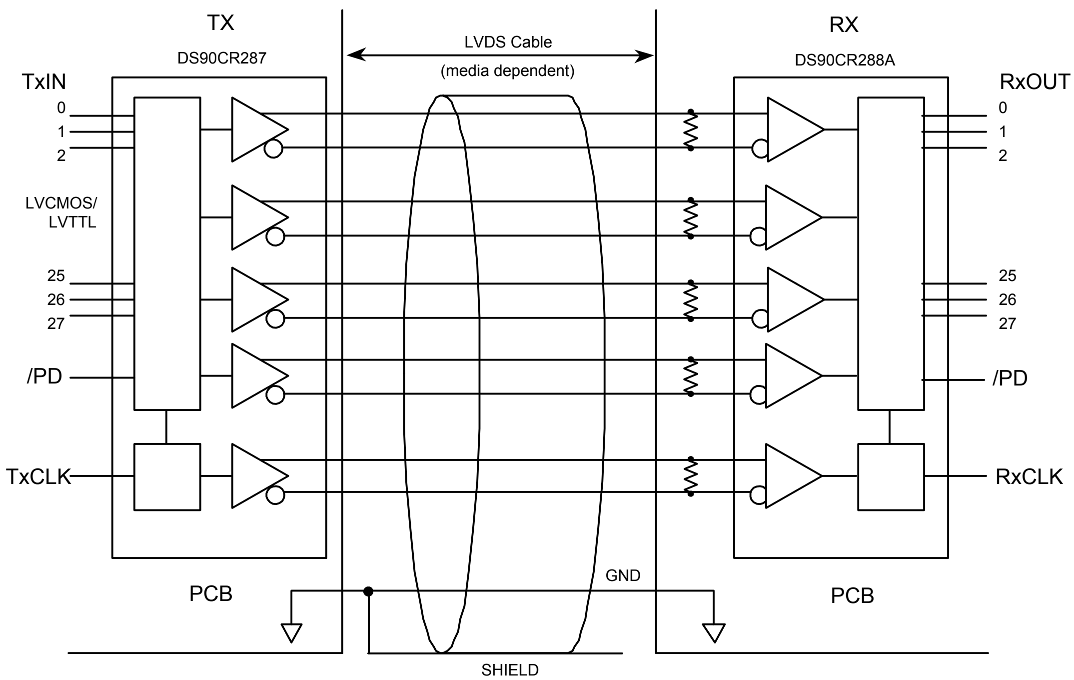
The Receiver board accepts the LVDS serialized data streams plus clock and converts the data back into parallel LVTTL/LVCMOS data signals and clock.

The user simply needs to provide the proper LVTTL/LVCMOS data input and clock to the Transmitter and the chipset will serialize, transmit, and deserialize the data converting it back into the LVTTL/LVCMOS parallel bus plus clock. A power down feature is also provided that reduces current draw when the link is not required.

Contents of the Evaluation Kit:

1) One Transmitter board with the DS90CR287MTD - 28 bit Transmitter
2) One Receiver board with the DS90CR288AMTD - 28 bit Receiver
3) One 2-meter Amphenol Spectra Strip Cable interface
4) One 60-pin IDC Flat Ribbon Cable
5) Evaluation Kit Documentation (this manual)
6) DS90CR287/288A Datasheet
7) Channel Link Application Notes AN-1041 and AN-1108

Channel Link Typical Application:



The diagram above illustrates the use of the Channel Link chipset (Tx/Rx). This chipset is able to transmit 28 bits of LVTTL/LVCMOS data using four LVDS channels for a total throughput of 2.38 Gbps (297.5 Mbytes/s).

Input clock rate is specified to be between 20 MHz to 85 MHz maximum. The interconnect between the two devices may be a variety of media including: twisted pair cables, twin-ax cables, and / or backplanes for example. Driving between the two devices is a function of interconnect skew and clock rate. Distances up to ten meters are possible at the lower clock rates and distances of 1 to 2 meters is possible at the higher clock rates. Please refer to the chipset datasheet for more information and parametric tables.

How to set up the Evaluation Kit:

The PCB routing for the Tx input pins (TxIN) have been laid out to accept incoming data from a 60-pin IDC connector. The TxOUT/RxIN interface uses the 3M MDR connector and Spectra Strip cable. This typical cable provides minimal skew between LVDS channels and can typically support longer lengths than atwisted pair cable. Please follow these steps to set up the evaluation kit for bench testing and performance measurements:

1) Connect one end of the Spectra Strip cable to the transmitter board and the other end to the receiver board. This is a standard pinout cable, longer lengths are available for purchase from Alliance Technology – see www.alliancet.com
2) Jumpers have been configured at the factory, they should not require any changes for operation of the chipset. See text on Jumper settings for more details.
3) For the incoming data, connect a flat (ribbon) cable to the transmitter board to a data source (signal generator, pattern generator, BERT tester, etc). Connect the 60-pin flat cable from the receiver board to the receiver load (BERT or other equipment). Scope probes may also be connected directly to the pins if desired. Mini-coax cable with headers on one end may also be used. This type of cable is supplied with some test equipment. The 60-pin IDC equipment interface cable is supplied with this kit which can be used to build custom cables.
4) Power for the Tx and Rx boards must be supplied externally through TP1 (Vcc). Grounds for both boards are connected through TP2 (GND) (see section below).
5) Data applied to the inputs is now serialized, transmitted, deserialized and re-driven at the receiver outputs.

This evaluation kit can also be used to evaluate the performance of other National Semiconductor’s 28-bit and 21-bit Channel Link Serdes chipset. Simply replace the existing DS90CR287/288A devices with a different 28-bit or 21-bit device chipset and follow the above procedure. For evaluation of 21-bit device chipset, user needs to pull TxIN[21:27] high or low.

Power Connection:

The Transmitter and Receiver boards must be powered by supplying power externally through TP1 (Vcc) and TP2 (GND) on EACH board. Information on maximum supply voltage can be found on device datasheet’s Absolute Maximum Ratings section. The maximum voltage that should ever be applied to the Channel Link Transmitter (DS90CR287) or Receiver (DS90CR288A) Vcc terminal is +4V MAXIMUM.

Channel Link Transmitter Board Description:

J1 (60 position) accepts 28 bit LVTTL/LVCMOS data, clock and also the PD* control signal.

The Channel Link Transmitter board is powered externally. For the transmitter to be operational, the Power Down pin must be set HIGH with a jumper.

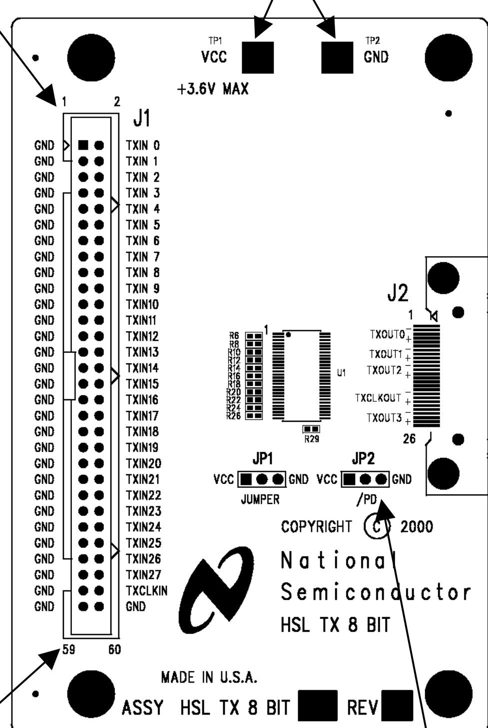
The 3M MDR connector (J2) provides the interface for LVDS signals for the Receiver board.

60-pin IDC Connector

J1

1	2
GND	**TXIN0**
GND	**TXIN1**
GND	**TXIN2**
GND	**TXIN3**
GND	**TXIN4**
GND	**TXIN5**
GND	**TXIN6**
GND	**TXIN7**
GND	**TXIN8**
GND	**TXIN9**
GND	**TXIN10**
GND	**TXIN11**
GND	**TXIN12**
GND	**TXIN13**
GND	**TXIN14**
GND	**TXIN15**
GND	**TXIN16**
GND	**TXIN17**
GND	**TXIN18**
GND	**TXIN19**
GND	**TXIN20**
GND	**TXIN21**
GND	**TXIN22**
GND	**TXIN23**
GND	**TXIN24**
GND	**TXIN25**
GND	**TXIN26**
GND	**TXIN27**
GND	**TXCLKIN**
GND	*GND*
59	60

Vcc and Gnd **MUST** be applied **externally** here



/PD

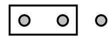
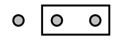
TxOUT LVDS signals
3M MDR connector

J2

Pin 1	Pin 14
NC	**OUT0-**
GND	**OUT0+**
NC	**NC**
OUT1-	**GND**
OUT1+	**NC**
OUT2-	**GND**
OUT2+	**NC**
NC	**NC**
NC	**CLK-**
GND	**CLK+**
NC	**NC**
OUT3-	**GND**
OUT3+	**NC**
Pin 13	Pin 26

Note: JP1 is not used

Jumper Settings for the Tx Board

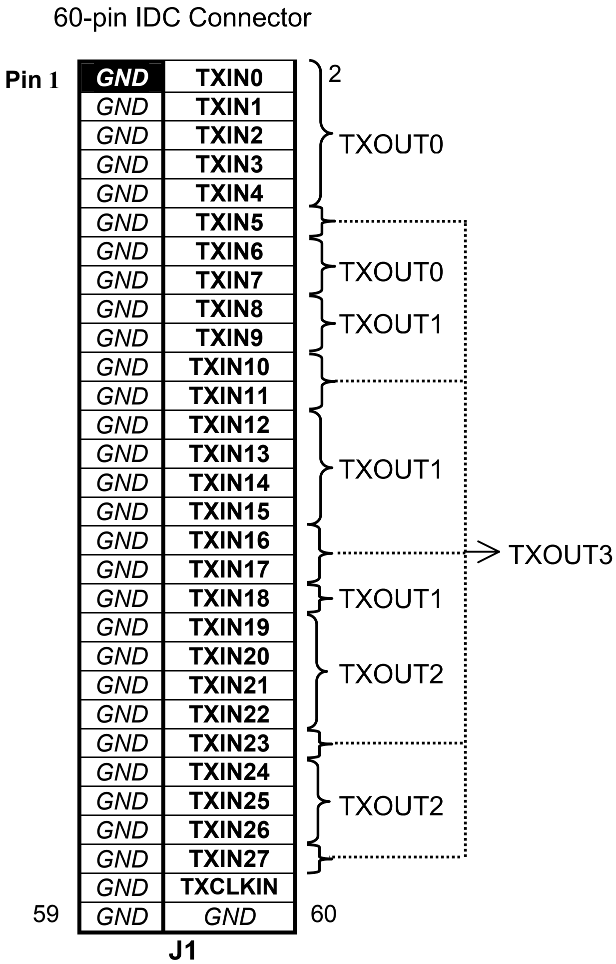
Jumper	Purpose	Settings	
/PD (JP2)	**P**ower**D**own	 = ON Vcc GND (ON: Tx is operational;	 = OFF Vcc GND OFF: Tx powers down)

Default setting is JP2 set HIGH (to Vcc), operational mode.

Tx LVDS Mapping by IDC Connector

The following two figures illustrate how the Tx inputs are mapped to the IDC connector (J1) (Note – labels are also printed on the demo boards). The 26-pin MDR connector pinout is also shown.

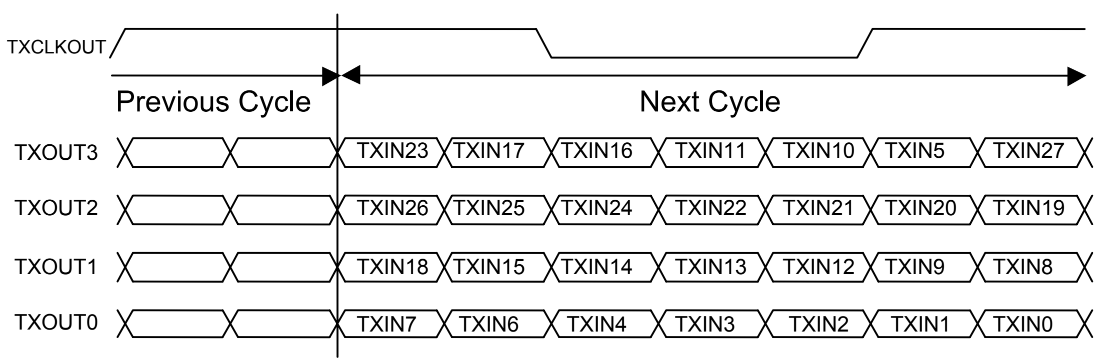
(Transmitter Board)



TxOUT LVDS signals
3M MDR connector

PIN #	NAME
1	***NC***
2	*GND*
3	***NC***
4	**OUT1-**
5	**OUT1+**
6	**OUT2-**
7	**OUT2+**
8	***NC***
9	***NC***
10	*GND*
11	***NC***
12	**OUT3-**
13	**OUT3+**
14	**OUT0-**
15	**OUT0+**
16	***NC***
17	*GND*
18	***NC***
19	*GND*
20	***NC***
21	***NC***
22	**CLK-**
23	**CLK+**
24	***NC***
25	*GND*
26	***NC***

J2



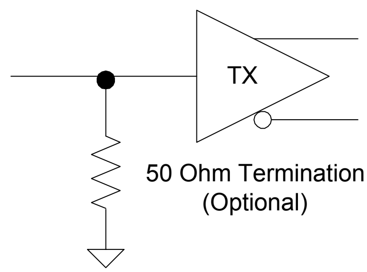
Parallel LVTTL/LVCMOS Data Inputs Mapped to LVDS Outputs

Tx Board Options: 50 Ohm Termination for TxIN

On the Tx demo board, the 29 inputs have an option for 50 Ohm terminations. There are 0402 pads for this purpose. One side is connected to the signal line and the other side is tied to ground. These pads are unpopulated from the factory but are provided if the user needs to install a 50 Ohm termination. R1 TO R28 are associated with the Tx data input lines. R29 is associated with CLKIN. Some test equipment may require a 50 Ohm load.

Mapping of Transmitter Inputs for the Optional Termination Resistors is shown below:

Tx Pin Names	Tx Pin Number	Termination Resistor
TxIN0	51	R1
TxIN1	52	R2
TxIN2	54	R3
TxIN3	55	R4
TxIN4	56	R5
TxIN5	2	R6
TxIN6	3	R7
TxIN7	4	R8
TxIN8	6	R9
TxIN9	7	R10
TxIN10	8	R11
TxIN11	10	R12
TxIN12	11	R13
TxIN13	12	R14
TxIN14	14	R15
TxIN15	15	R16
TxIN16	16	R17
TxIN17	18	R18
TxIN18	19	R19
TxIN19	20	R20
TxIN20	22	R21
TxIN21	23	R22
TxIN22	24	R23
TxIN23	25	R24
TxIN24	27	R25
TxIN25	28	R26
TxIN26	30	R27
TxIN27	50	R28
TxCLKIN	31	R29



BOM (Bill of Materials) Transmitter PCB:

HSL Demo Board Schematic REV1
HSL8TXR1 Revision: 1 Channel Link

Item	Qty	Reference	Part	Pkg Size
1	1	C1	10 µF	CASE D
2	4	C2,C6,C10,C14	0.1 µF	1206 (3216)
3	4	C3,C7,C11,C15	22 µF	7343 (D)
4	3	C4,C8,C12	0.001 µF	0805 (2012)
5	3	C5,C9,C13	0.01 µF	0805 (2012)
6	2	JP2	3_PIN_HEADER	0.1" spacing
7	1	J1	IDC30X2	IDC60
8	1	J2	3M_MDR	26MDR
9	29	R1,R2,R3,R4,R5,R6,R7,R8, R9,R10,R11,R12,R13,R14, R15,R16,R17,R18,R19,R20, R21,R22,R23,R24,R25,R26, R27,R28,R29	Optional	0402 PAD
10	8	R30,R32,R33,R34,R35, R36,R37	0 Ohm	0402
11	2	TP1,TP2	N/A	TP_.2"X.2"
12	1	U1	DS90CR287MTD	56-pin TSSOP

Rx Channel Link Receiver Board:

J1 (60 position) provides access to the 28 bit LVTTL/LVCMOS, clock outputs.

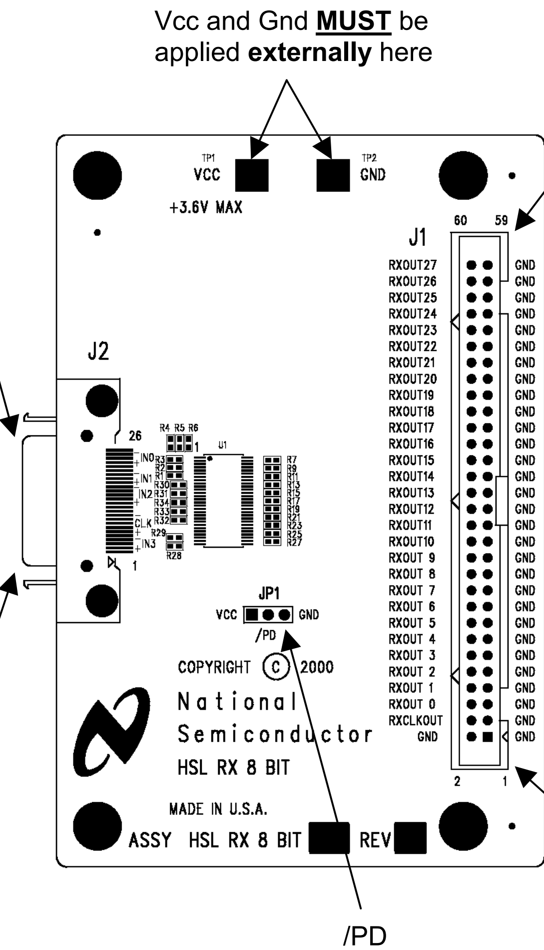
The Channel Link Receiver board is powered from the pads show below. For the receiver to be operational, the Power Down pin must be set HIGH with the jumper.

The 3M MDR connector (J2) provides the interface for LVDS signals for the Receiver board.

RxIN LVDS signals
3M MDR26-7 connector

J2 (Pin 26 / Pin 13 at top, Pin 14 / Pin 1 at bottom)

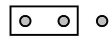
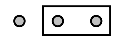
NC	IN0-
GND	IN0+
NC	NC
IN1-	GND
IN1+	NC
IN2-	GND
IN2+	NC
NC	NC
NC	CLK-
GND	CLK+
NC	NC
IN3-	GND
IN3+	NC



J1 (pins 60/59 at top, 2/1 at bottom)

60	59
RXOUT27	*GND*
RXOUT26	*GND*
RXOUT25	*GND*
RXOUT24	*GND*
RXOUT23	*GND*
RXOUT22	*GND*
RXOUT21	*GND*
RXOUT20	*GND*
RXOUT19	*GND*
RXOUT18	*GND*
RXOUT17	*GND*
RXOUT16	*GND*
RXOUT15	*GND*
RXOUT14	*GND*
RXOUT13	*GND*
RXOUT12	*GND*
RXOUT11	*GND*
RXOUT10	*GND*
RXOUT9	*GND*
RXOUT8	*GND*
RXOUT7	*GND*
RXOUT6	*GND*
RXOUT5	*GND*
RXOUT4	*GND*
RXOUT3	*GND*
RXOUT2	*GND*
RXOUT1	*GND*
RXOUT0	*GND*
RXCLKOUT	*GND*
GND	***GND***
2	1

Selectable Jumper Settings for the Rx Board

Jumper	Purpose	Settings	
/PD (JP1)	**P**ower**D**own	 = ON Vcc GND (ON: Rx is operational;	 = OFF Vcc GND OFF: Rx powers down)

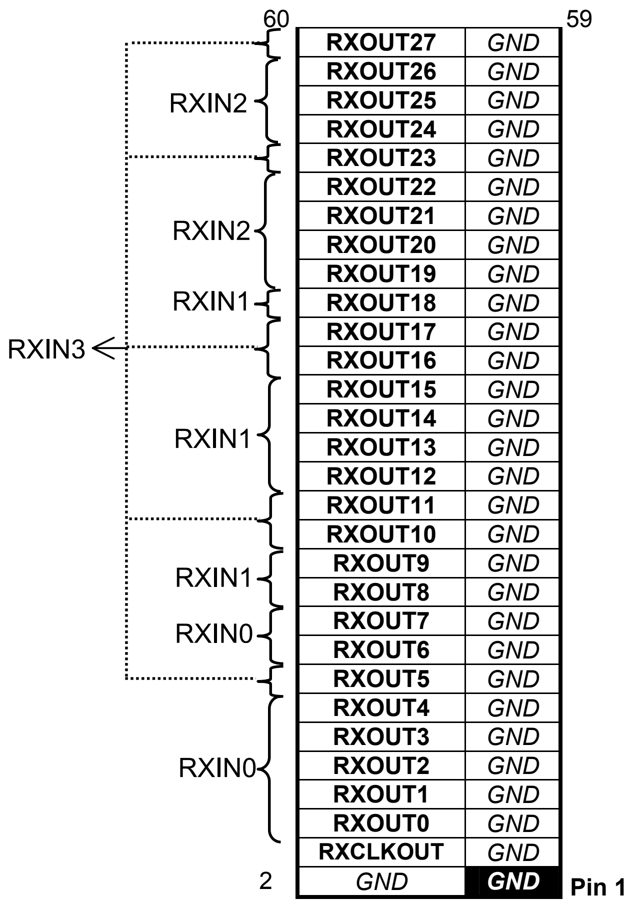
Default setting is JP1 set HIGH (to Vcc), operational mode.

LVDS Mapping by IDC Connector

The following two figures illustrate how the Rx outputs are mapped to the IDC connector (J1) (Note – labels are also printed on the demo boards). The 26-pin MDR connector pinout is also shown.

(Receiver Board)

60-pin IDC Connector

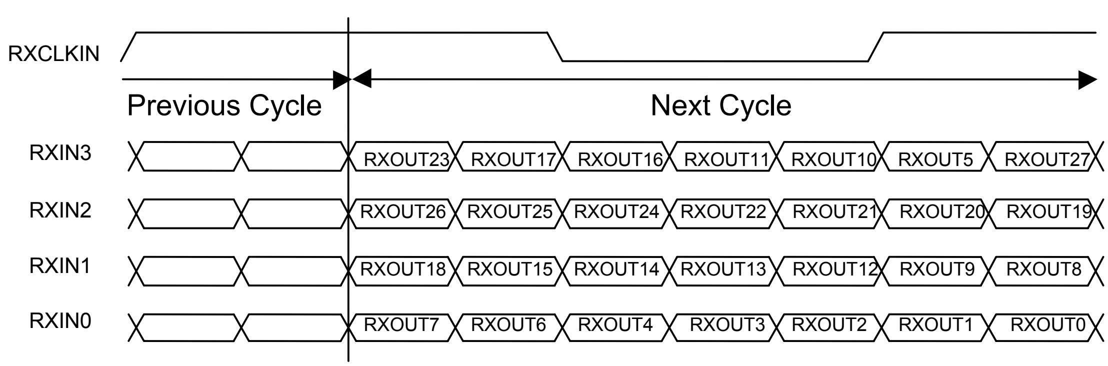


J1

RxIN LVDS signals
3M MDR connector

PIN #	NAME
1	***NC***
2	*GND*
3	***NC***
4	**CLK+**
5	**CLK-**
6	***NC***
7	***NC***
8	*GND*
9	***NC***
10	*GND*
11	***NC***
12	**IN0+**
13	**IN0-**
14	**IN3+**
15	**IN3-**
16	***NC***
17	*GND*
18	***NC***
19	***NC***
20	**IN2+**
21	**IN2-**
22	**IN1+**
23	**IN1-**
24	***NC***
25	*GND*
26	***NC***

J2



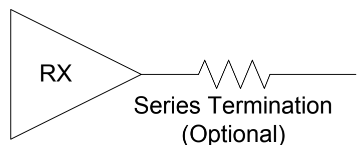
LVDS Data Inputs Mapped to LVTTL/LVCMOS Outputs

Rx Optional: Series Termination for RxOut

On the Rx demo board, there are 29 outputs that have an 0402 pad in series (which are shorted out). These pads are unpopulated from the factory but are provided if the user needs to install a 450 Ohm series resistors. This is required if directly connecting to 50 Ohm inputs on a scope. To use this option the user must cut the signal line between the pads before installing the 450 Ohm series resistors. R1 to R28 are associated with the DATA output lines. R29 is associated with CLKOUT. The total load presented to the receiver output is 500 Ohms (450 + 50). The waveform on the scope is 1/10 of the signal due to the resulting voltage divider (50 / (450 + 50)).

Optional Series Termination Resistor mapping is shown below:

Rx Pin Names	Rx Pin Number	Series Termination Resistor
RxOUT0	27	R28
RxOUT1	29	R27
RxOUT2	30	R26
RxOUT3	32	R25
RxOUT4	33	R24
RxOUT5	34	R23
RxOUT6	35	R22
RxOUT7	37	R21
RxOUT8	38	R20
RxOUT9	39	R19
RxOUT10	41	R18
RxOUT11	42	R17
RxOUT12	43	R16
RxOUT13	45	R15
RxOUT14	46	R14
RxOUT15	47	R13
RxOUT16	49	R12
RxOUT17	50	R11
RxOUT18	51	R10
RxOUT19	53	R9
RxOUT20	54	R8
RxOUT21	55	R7
RxOUT22	1	R6
RxOUT23	2	R5
RxOUT24	3	R4
RxOUT25	5	R3
RxOUT26	6	R2
RxOUT27	7	R1
RxCLKOUT	26	R29



BOM (Bill of Materials) Receiver PCB:

HSL Demo Board Schematic REV1
HSL8RXR1 Revision: 1 Channel Link

Item	Qty	Reference	Part	Pkg Size
1	1	C1	10 µF	CASE D
2	4	C2,C6,C10,C14	0.1 µF	1206 (3216)
3	4	C3,C7,C11,C15	22 µF	7343 (D)
4	3	C4,C8,C12	0.001 µF	0805 (2012)
5	3	C5,C9,C13	0.01 µF	0805 (2012)
6	1	JP1	3_PIN_HEADER	0.1" spacing
7	1	J1	IDC30X2	IDC60
8	1	J2	3M_MDR	26MDR
9	29	R1,R2,R3,R4,R5,R6,R7,R8, R9,R10,R11,R12,R13,R14, R15,R16,R17,R18,R19,R20, R21,R22,R23,R24,R25,R26, R27,R28,R29	Optional (See previous page)	0402 PAD
	6	R35,R36,R37,R38,R39,R40	0 Ohm	0402
10	5	R30,R31,R32,R33,R34	100 Ohm	0402
11	2	TP1,TP2	N/A	TP_.2"X.2"
12	1	U1	DS90CR288AMTD	56-pin TSSOP

Typical Connection / Test Equipment

The following is a list of typical test equipment that may be used to generate signals for the TX inputs:

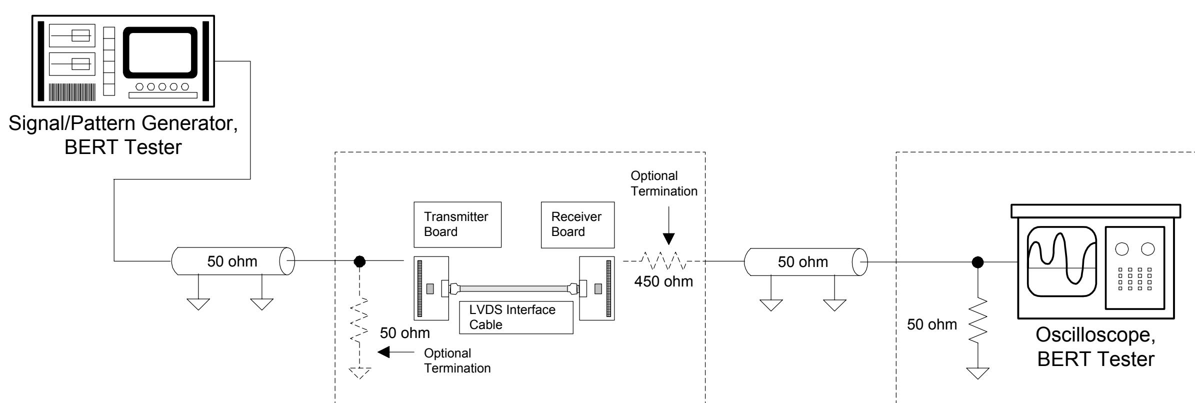
1) TEK HFS9009 - This pattern generator along with 9DG2 Cards may be used to generate input signals and also the clock signal.
2) TEK DG2020 - This generator may also be used to generate data and clock signals.
3) TEK MB100 BERT - This bit error rate tester may be used for both signal source and receiver.
4) Any other signal / pattern generator that generates the correct input levels as specified in the datasheet.

The following is a list of typically test equipment that may be used to monitor the output signals from the RX:

1) TEK MB100 BERT - Receiver.
2) Any SCOPE with 50 Ohm inputs or high impedance probes.

LVDS signals may be easily measured with high impedance / high bandwidth differential probes such as the TEK P6247 or P6248 differential probes.

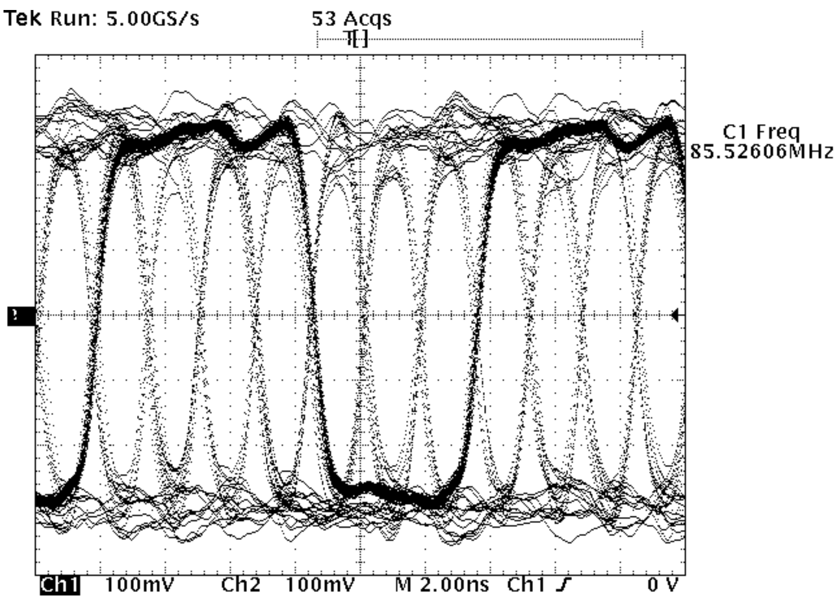
The picture below shows a typical test set up using a generator and scope.



Typical Connection / Test Equipment Setup

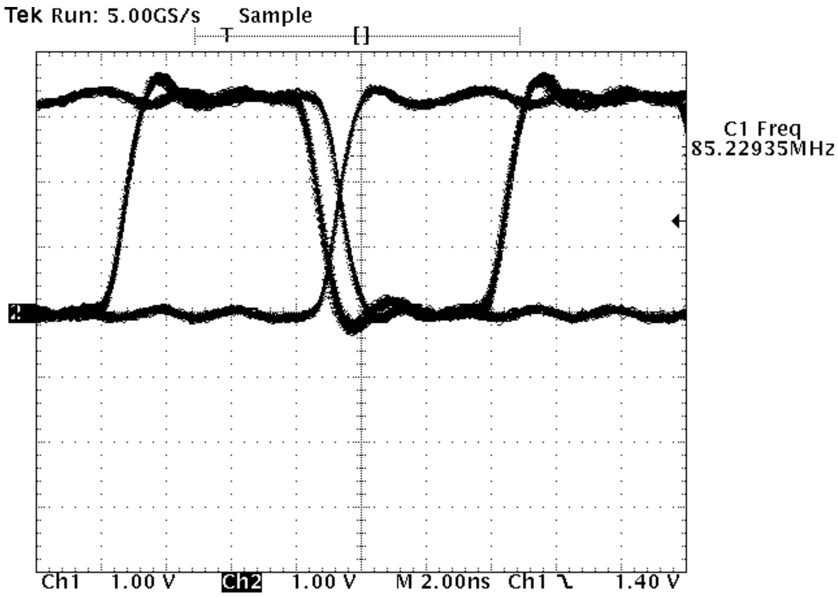
Typical Waveshapes

LVDS



The plot above shows both the LVDS Data channel with PRBS data and also the LVDS Clock over laid. Note that the clock pattern is 4 bit times HIGH and 3 bit times LOW. The differential signal should be typically +/-300mV. These waveforms were acquired using the TEK P6248 Probes. Clock rate is 85MHz.

RxOUT



The plot above shows both the recovered PRBS data and also the regenerated Clock overlaid. Note that the clock transitions slightly before the data transition and strobes the data on the rising edge of the clock. The data and clock signals are low drive 3V CMOS outputs. The plot above is at 85MHz.

Troubleshooting

If the demo boards are not performing properly, use the following as a guide for quick solutions to potential problems. If the problem persists, please contact the Interface Applications hotline number (+1 408 721 8500) for assistance.

QUICK CHECKS:
1. Check that Power and Ground are connected to both Tx AND Rx boards.
2. Check the supply voltage (typical 3.3V) and also current draw with both Tx and Rx boards (should be about 200mA with clock and one data bit at 66MHz).
3. Verify input clock and input data signals meet requirements (VIL, VIH, tset, thold), Also verify that data is strobed on the rising edge of the clock.
4. Check that the Jumpers are set correctly.
5. Check that the 2 meter cable is properly connected.

TROUBLESHOOTING CHART

Problem…	**Solution…**
There is only the output clock. There is no output data.	Make sure the data is applied to the correct input pin. Make sure data is valid at the input.
No output data and clock.	Make sure Power is on. Input data and clock are active and connected correctly. Make sure that the 2 meter cable is secured to both demo boards.
Power, ground, input data and input clock are connected correctly, but no outputs.	Check the Power Down pins of both boards and make sure that the devices are enabled (/PD=Vcc) for operation.
The devices are pulling more than 1A of current.	Check for shorts in the cables connecting the TX and RX boards.
After powering up the demo boards, the power supply reads less than 3V when it is set to 3.3V.	Use a larger power supply that will provide enough current for the demo boards, a 500mA power supply is recommended.

Additional Information

For more information on Channel Link Transmitters/Receivers, refer to the National's LVDS website at:

www.national.com/appinfo/lvds

Application Notes

- AN-1041 Channel Link Moving and Shaping Information in Point-to-Point Applications
- AN-971 An Overview of LVDS technology
- AN-977 LVDS Signal Quality: Jitter Measurement Using Eye Pattern
- AN-1059 High Speed Transmission with LVDS Devices
- AN-1108 Channel-Link PCB and Interconnect Design-In Guidelines

Interface Applications Hotline:

The Interface Hotline number is: +1 408 721-8500

Appendix

Cable and connector

The next few pages provide a full description of the cable and connector.
For product request please contact 3M and Alliance Technology Enterprise.

3M Connector Data is available at: www.mmm.com/Interconnects
Spectra Strip Cable Data is available at: www.alliancet.com

Tx PCB Schematic

Transmitter Board: HSL Demo Board Schematic
Document Number: HSL8TX
Rev: 1.0

Rx PCB Schematic

Receiver Board: HSL Demo Board Schematic
Document Number: HSL8RX
Rev: 1.0

.050″ Mini D Ribbon (MDR) Connectors

Surface Mount Right Angle Receptacle — Shielded 102XX-1210VE Series



140

IMPORTANT NOTICE TO PURCHASER

TS-0755-05
Date Issued: February 5, 1998

Physical

Insulation
Material: Glass Reinforced Polyester (PCT)
Flammability: UL 94V-0
Color: Beige

Contact
Material: Copper Alloy (C521)
Plating
Underplate: 80 μ″ [2.0 μm] Nickel — QQ-N-290, Class 2
Wiping Area: 20 μ″ [0.50 μm] Min Gold — MIL-G-45204, Type II, Grade C

Shroud and Latch Hook
Material: Steel
Plating: Nickel

Screw Lock
Material: Copper Alloy (C521)
Plating: Tin

Marking: 3M Logo and Part Number

Electrical

Current Rating: 1 A
Insulation Resistance: $> 5 \times 10^8 \Omega$ at 500 VDC
Withstanding Voltage: 500 Vrms for 1 Minute

Environmental

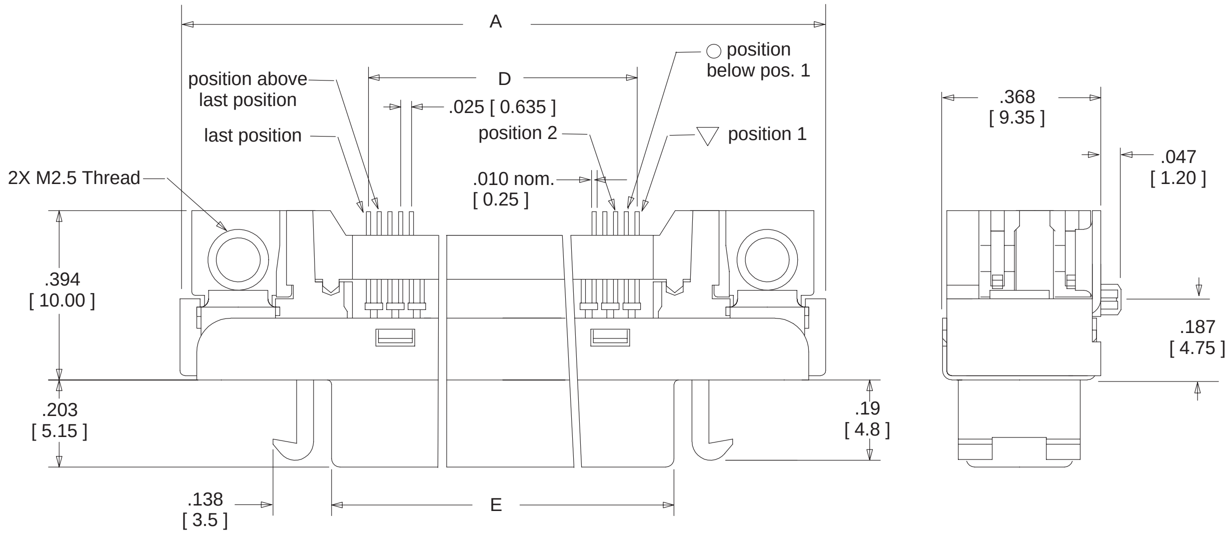
Temperature Rating: –55°C to +105°C
Process: Surface mount compatible up to 240°C peak for short durations.

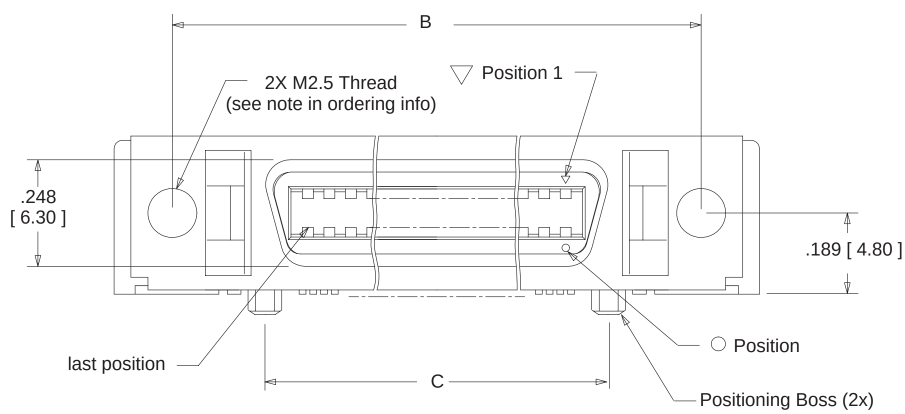
UL File No.: E68080

3M Electronic Products Division
6801 River Place Blvd.
Austin, TX 78726-9000

For technical, sales or ordering information call
800-225-5373

Contact Quantity	3M Part Number	Dimensions				
		A±.008	B±.006	C±.006	D±.006	E±.006
20	**10220-1210 VE**	1.32 [33.4]	1.081 [27.45]	.650 [16.51]	.475 [12.07]	.646 [16.4]
26	**10226-1210 VE**	1.50 [38.2]	1.231 [31.26]	.800 [20.32]	.625 [15.88]	.795 [20.2]
40	**10240-1210 VE**	1.85 [47.1]	1.581 [40.15]	1.150 [29.21]	.975 [24.77]	1.150 [29.2]





Inch
[mm]

Tolerance Unless Noted			
	.0	.00	.000
Inch	± .1	± .01	± .005

[ ] Dimensions for Reference only

Ordering Information

102XX-1210VE

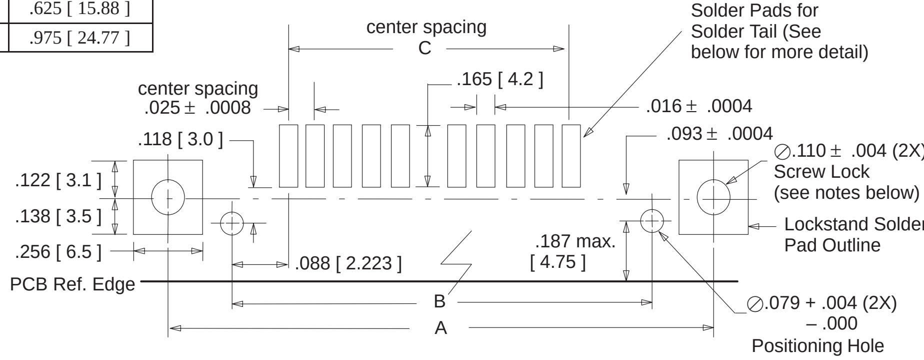
Contact Quantity (See Table)

Note: Use (M2.5x8mm) screws to mount to panel with max. thickness of 2.0 mm.

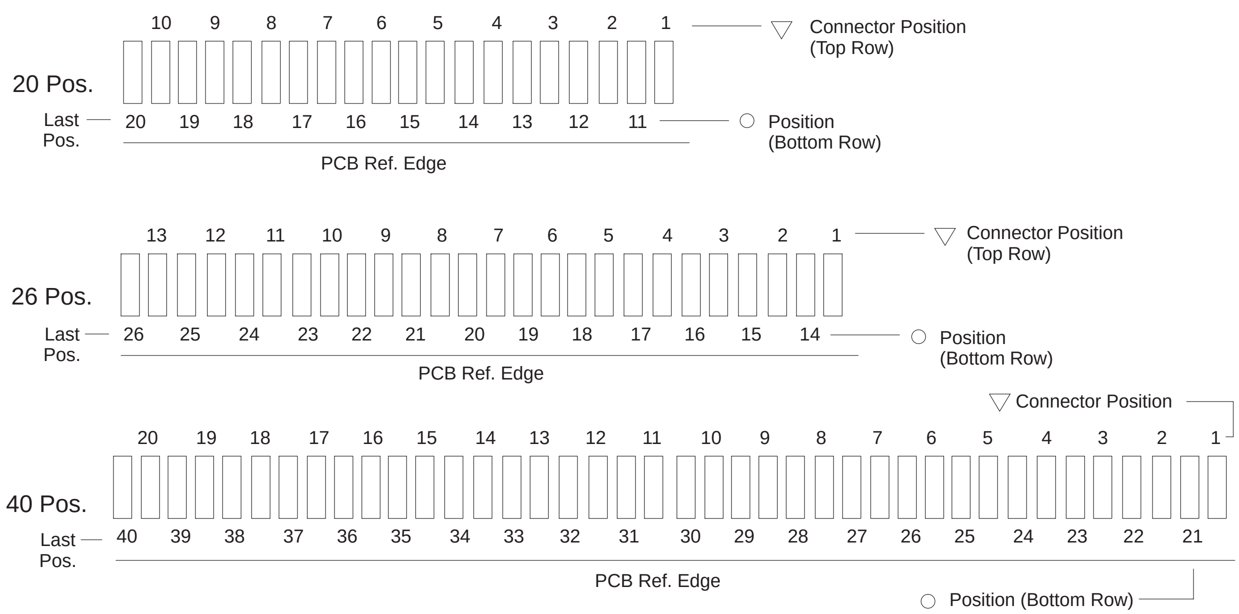
TS-0755-05
Sheet 2 of 3

Contact Quantity	Dimensions		
	A ± .002	B ± .002	C ± .002
20	1.081 [27.45]	.650 [16.51]	.475 [12.07]
26	1.230 [31.26]	.800 [20.32]	.625 [15.88]
40	1.581 [40.15]	1.150 [29.21]	.975 [24.77]

Recommended Board Layout
(viewed from connector side)

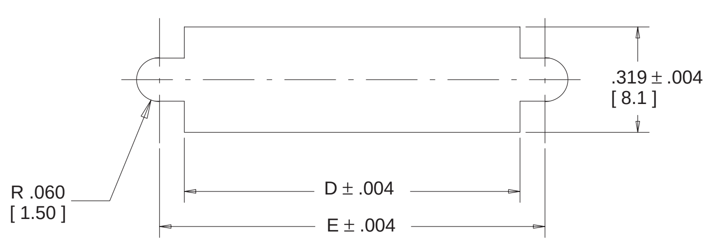


Solder Tail Layout Detail
(#'s Correspond to Connector Contact # Shown on Previous Page)



Contact Quantity	Dimensions	
	D	E
20	.94 [23.8]	1.081 [27.45]
26	1.09 [27.6]	1.231 [31.26]
40	1.44 [36.5]	1.581 [40.15]

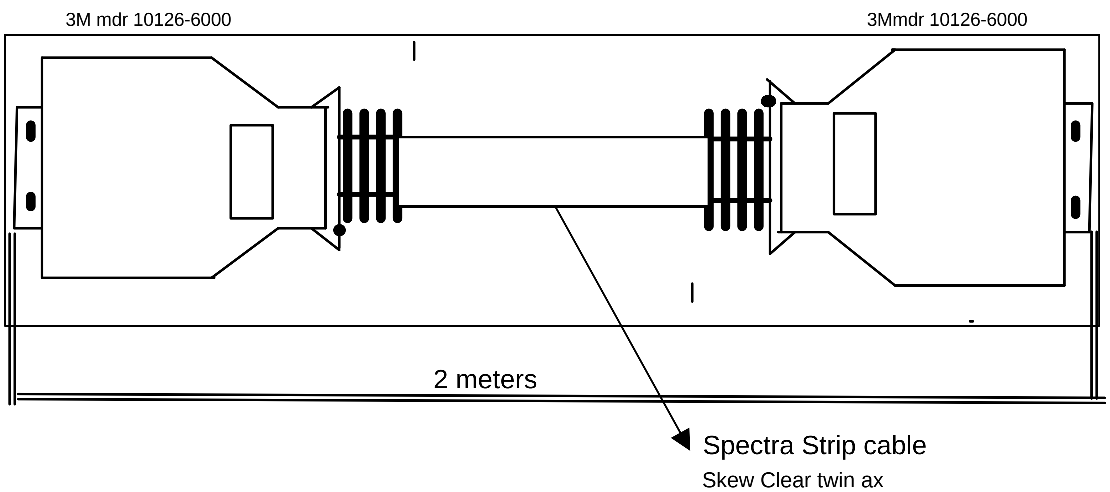
Recommended Panel Cut-out
Note: Panel thickness .079 [2.00] Max.



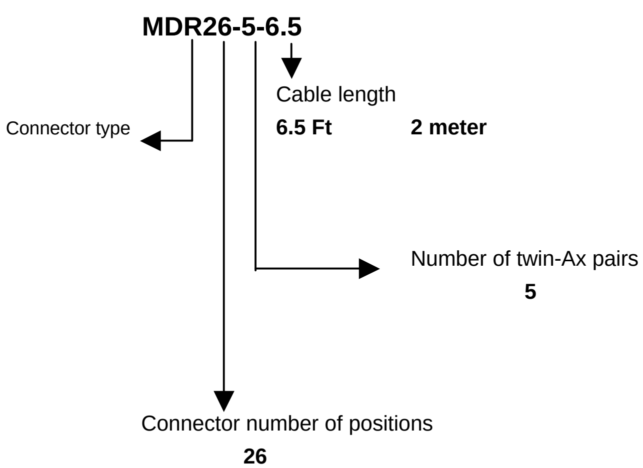
**Notes:
1. Plated through holes for .062″ board thickness.
2. Use mounting screws (M2.5) to fasten to board.

TS-0755-05
Sheet 3 of 3

Cable Assembly Part number   MDR26-5-6.5



Part number



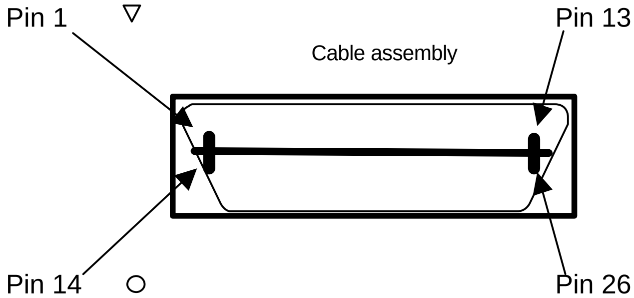
Cable assemby ordering information.

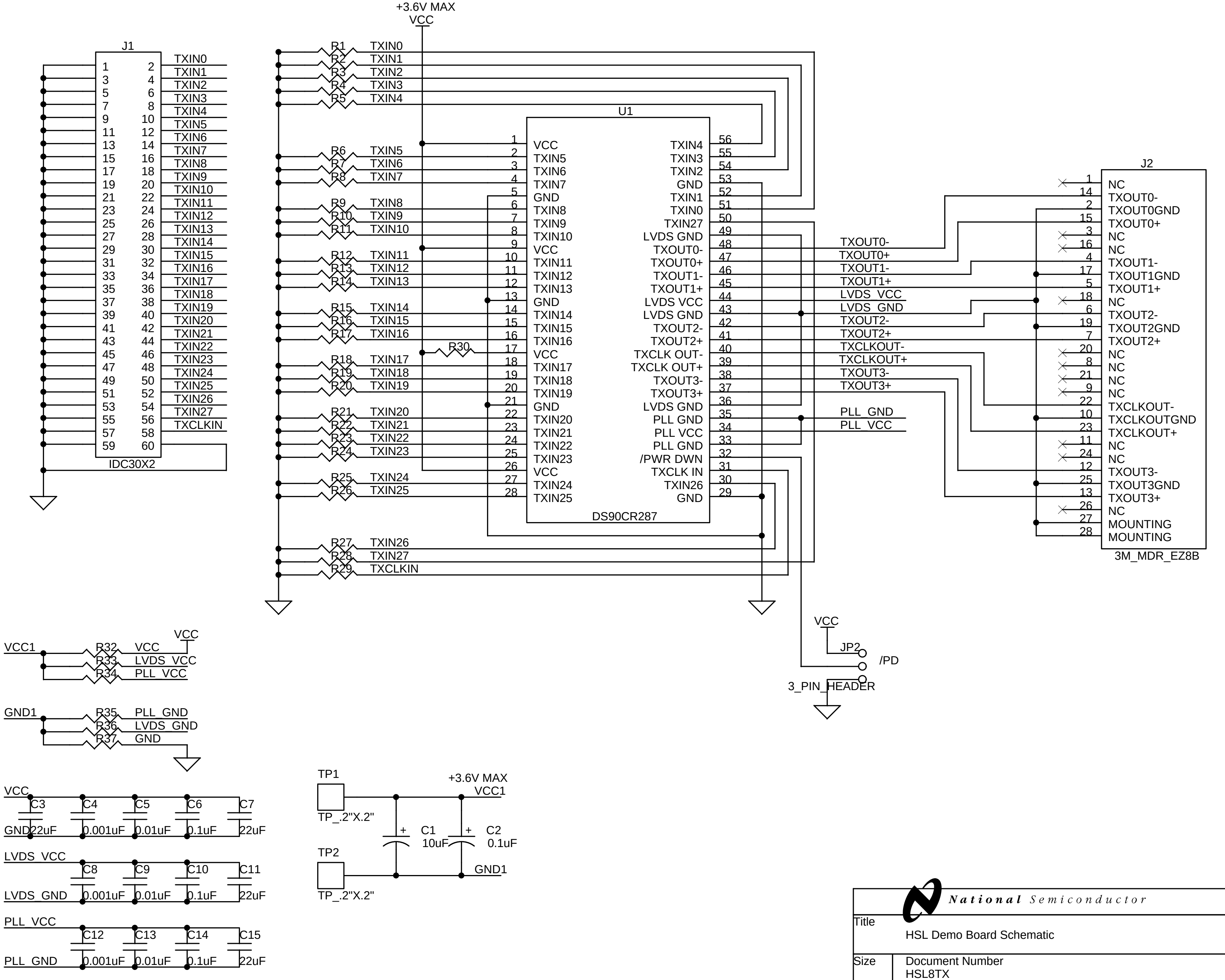
Alliance Technology Enterprise
521 Central Ave Suite B
Menlo Park CA 94025
650 329 8554
info@allianceT.com
www.AllianceT.com

National Semiconductor Channel Link Cable Assembley Pinout

Alliance Technology part number MDR26-5-6.5C

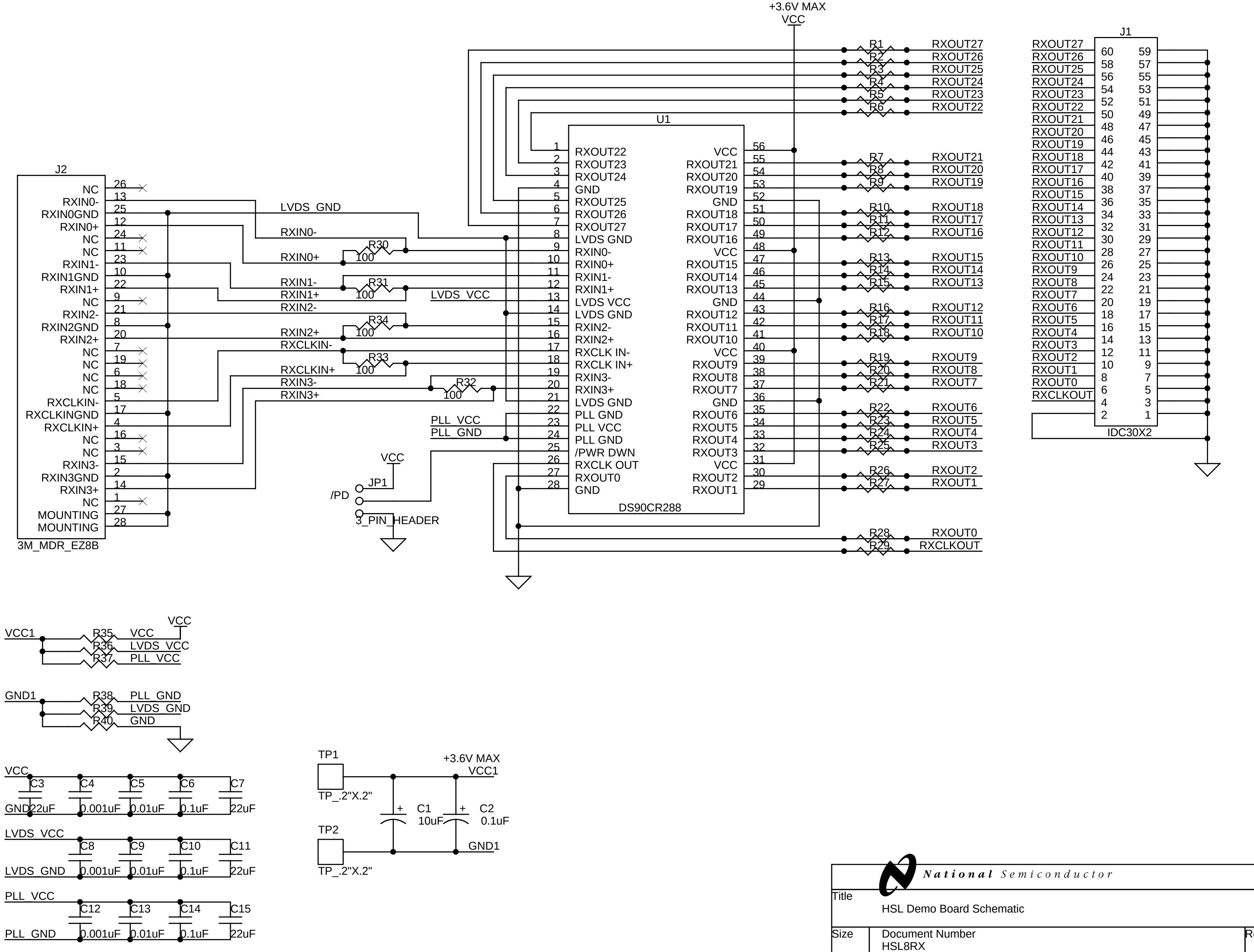
Pin Assignment **Side A** 3M Mdr Part 10126-6000		Pin Assignment Side B 3M Mdr Part 10126-6000	
1	No Connect	26	No Connect
2	TxOut0Gnd+	25	TxOutGnd-
3	No Connect	24	No Connect
4	TxOut1-	23	RxIn1 -
5	TxOut1+	22	RxIn1 +
6	TxOut2-	21	RxIn2 -
7	TxOut2+	20	RxIn2 +
8	Reserved	19	Reserved
9	No Connect	18	No Connect
10	TxClkoutGnd	17	RxInClkGnd
11	No Connect	16	No Connect
12	TxOut3-	15	RxIn3 -
13	Txout3+	14	Rxin3 +
14	TxOut0-	13	RxIn0 -
15	TxOut0+	12	Rxin0 +
16	No Connect	11	No Connect
17	TxOut1Gnd	10	RxIn1Gnd
18	No Connect	9	No Connect
19	TxOut2gnd	8	Rxin2Gnd
20	Reserved	7	Reserved
21	Reserved	6	Reserved
22	TxClkOut-	5	RxClkIn -
23	TxClkOut+	4	RxClkIn +
24	No Connect	3	No Connect
25	TxOut3Gnd	2	RxIn3Gnd
26	No Connect	1	No Connect





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Title	HSL Demo Board Schematic	
Size	Document Number HSL8TX	Rev 1
Date: Monday, August 21, 2000	Sheet 1 of 1	



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Title	HSL Demo Board Schematic	
Size	Document Number HSL8RX	Rev 1
Date: Monday, August 21, 2000	Sheet 1 of 1	

IMPORTANT NOTICE

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

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